IN THE CLAIMS

Please ~~amend the~~ claims as follows:

Claim 1 (Currently Amended): Synchronization circuit for processing an external sequence of analog values which is derived from an input sequence, <u>the circuit</u> comprising<u>:</u>

an analog feedback shift register ~~(1)~~<u>including a shift register having memory locations configured to store</u> ~~, in which~~ analog values ~~stored in memory locations of a shift register (6)~~ <u>that</u> are combined according to a specific feedback pattern ~~for deriving~~ <u>to produce</u> a feedback value according to a feedback function, from which a new input value is generated by superposition with a new element of the external sequence, ~~which~~ <u>the new</u> input value is fed to the input of the shift register ~~(6)~~, ~~characterized in that~~ <u>and</u> the feedback function is substantially a linear combination of ~~the~~ arguments ~~within substantially each sector characterized by specific values of the signs of the arguments~~ <u>associated with each of plural sectors, wherein each of the plural sectors is a portion of an argument space in which the signs of the arguments have predetermined values</u>.

Claim 2 (Currently Amended): Synchronization circuit according to Claim 1, ~~characterized in that~~ <u>wherein</u> the magnitude of the feedback function is 1 if the magnitudes of the arguments are each 1.

Claim 3 (Currently Amended): Synchronization circuit according to Claim 1 or 2, ~~characterized in that~~ <u>wherein</u> the sign of the feedback function always corresponds to the sign of the combination of the arguments.

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Claim 4 (Currently Amended): Synchronization circuit according to ~~any of Claims~~ Claim 1 ~~to 3~~, ~~characterized in that~~ wherein the feedback function is invariant when the arguments are interchanged.

Claim 5 (Currently Amended): Synchronization circuit according to ~~any of Claims~~ Claim 1 ~~to 4~~, ~~characterized in that~~ wherein the feedback function as a function of each argument is antisymmetrical and monotonic.

Claim 6 (Currently Amended): Synchronization circuit according to Claim 1, ~~characterized in that~~ wherein the magnitude of the feedback function substantially corresponds to the mean value of the magnitudes of the arguments.

Claim 7 (Currently Amended): Synchronization circuit according to ~~any of Claims~~ Claim 1 ~~to 6~~, ~~characterized in that~~ wherein the feedback value is produced by multiplying the value of the feedback function by a factor k<1, which is preferably between 0.90 and 0.99.

Claim 8 (Currently Amended): Synchronization circuit according to ~~any of Claims~~ Claim 1 ~~to 7~~, ~~characterized in that it comprises~~ further comprising a feedback circuit ~~(7) for evaluating~~ configured to evaluate the feedback function and a gain block ~~(8)~~ for multiplying ~~its~~ an initial value of the feedback circuit with a factor and an adder ~~(5) for superposing~~ configured to superpose the factor multiplied initial feedback value with a new element of the external sequence.

Claim 9 (Currently Amended): Synchronization circuit according to Claim 8, ~~characterized in that it comprises~~ further comprising a discriminator ~~(9) for generating~~

configured to generate a binary output signal indicating completed synchronization, the input

of which is connected to the output of the feedback circuit (7) and which preferably

comprises a squaring circuit or another circuit mapping an input signal into the positive

domain, a low-pass filter and a threshold value detector.

Claim 10 (Currently Amended): Synchronization circuit according to ~~any of Claims~~

Claim 1 ~~to 9, characterized in that it has~~ further comprising a buffer (2) in front of the analog

feedback shift register ~~(1) for adding,~~ the buffer configured to add successive segments of an

input sequence, each of which contains a fundamental sequence, ~~for generating the external~~

~~sequence~~.

Claim 11 (Currently Amended): Synchronization circuit according to Claim 10,

~~characterized in that~~ wherein the buffer comprises a shift register (4) and an adder (3) in front

of ~~it for adding~~ the shift register, the adder configured to add a member of the input sequence

to an output value of the shift register (4).